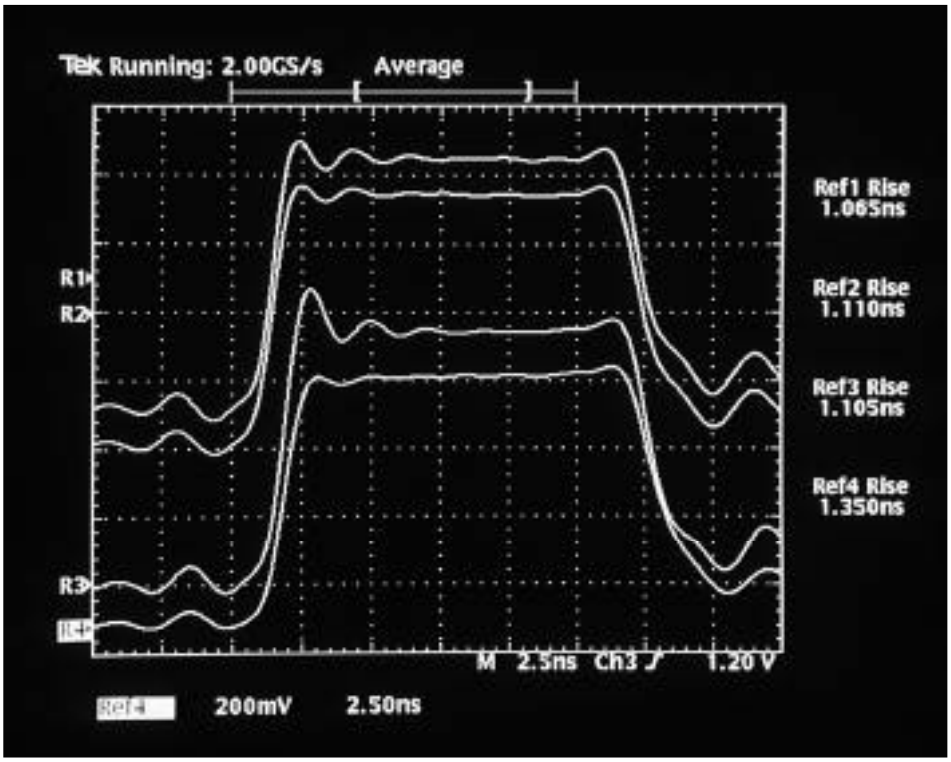
Tektronix

Technical Brief

The Effect of Probe Input Capacitance On Measurement Accuracy



Probing an ECLcircuit with series termination using a passive probe (trace T3 and T4) and an active FET probe (traces T1 and T2).

Introduction

High-performance logic families have pushed the world of CMOS and ECL into the picosecond realm. When output transitions move into this time domain, it becomes necessary to critically analyze signal measurements made with a probe.

Oscilloscope users need to consider these questions:

- How much, if any, does probe input capacitance affect the measured signal?
- How much capacitance can be tolerated? Do I need to be concerned about this?

Selecting a probe with the right capacitance will significantly improve measurement accuracies.

Most digital and analog designers agree that an increasingly important consideration in selecting a probe is capacitance. The capacitance of the probe or fixture adds to the load of the device-under-test (DUT) and can cause the risetime to be degraded or induce aberrations such as ringing in the acquired signal. In cases where high-impedance probing is required due to circuit loading considerations, probe capacitance is especially important. Probe capacitance not only loads the circuit, but it increases the need for careful grounding.

Just as bandwidth and risetime of an oscilloscope can have a significant impact on making accurate timing and amplitude measurements, capacitance of a probe can substantially alter a measured waveform's risetime and waveshape. In digital systems, clock rate is not the determining factor of the scope's bandwidth requirement. Clock rate is not the critical determinant in choosing probe input capacitance values either. Instead, the rise and fall times of the signals to be measured are the appropriate factors for selecting both the scope bandwidth **and** probe input capacitance.

It's important to keep in mind the relationship between risetime (tr) and bandwidth when you are choosing an oscilloscope and/or probe to make precise timing measurements:

$$bw_{(-3dB)} \approx 0.35/tr$$

Similarly, probe input capacitance directly influences the fastest signal components within the DUT. Don't use the clock rate as the determining component for choosing input capacitance of a probe, since it's usually much lower than the bandwidth of the signals due to their fast edges. Work station computers, for example, which often employ Advanced CMOS logic running at clock rates up to 300 MHz usually have signal rise times with bandwidths of 700 MHz and more.

For additional information on making an informed choice about oscilloscope and/or probe bandwidth as it relates to measurement error, obtain a copy of Tektronix technical brief 85W-8907-0, "*The Effect of Bandwidth on*

Table 1. Typical Logic Technology Risetimes and Equivalent Bandwidths with Typical Gate Input Capacitance

Logic Family	Rise time	Typical Bandwidth (–3 dB)	Gate Input Capacitance
CMOS	1.5 nsec	230 MHz	5 pF
Advanced CMOS	800 psec	440 MHz	3 pF
ECL	500 psec	700 MHz	3 pF
ECLipse	300 psec	1.17 GHz	1.4 pF
GaAs	100 psec	3.5 GHz	1.5 pF

Measurement Accuracy" and technical brief 60W-8412-1, "*Probing High Frequency Digital Circuitry*".

The Effect of Probe Input Capacitance

When the load capacitance of the probe you are using is significant compared to the capacitive load the DUT is designed to drive, your chance of making an accurate measurement is substantially reduced. Remember that the total capacitive loading for a DUT is a combination of the designed-for capacitive fanout, environmental capacitance, and the probe input capacitance. The ratio of the probe capacitance to the DUT capacitance alters the original waveform geometry in both the vertical axis as well as the horizontal axis by that ratio.

The DC loading fanouts for logic circuits are computed by dividing the output current by the input current. However, both AC limitations and current needed in the output termination can be expected to restrict the DUT fanout to a smaller number than the one computed. If the maximum number of permissible fanout loads are not exceeded by the addition of some amount of probe input capacitance beyond a good safety margin, then it's safe to assume that the probe will not appreciably invade the DUT output waveform. And, correspondingly, the measured waveform accurately represents the DUT output as if the probe capacitance were not there. This is the ideal case. The digital designer must verify that probe input capacitance is within the device fanout load specification and, therefore, causes minimum signal distortion and maximum signal fidelity.

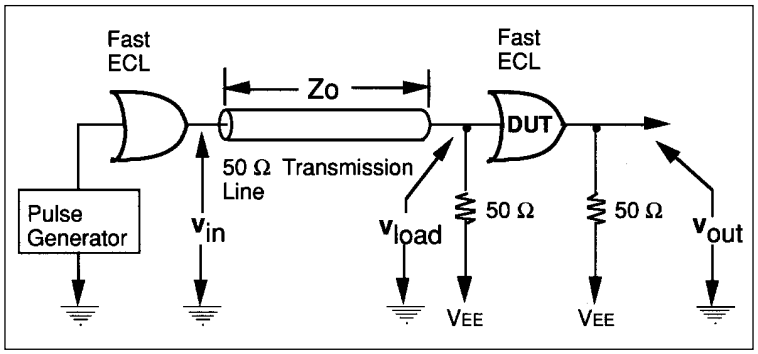


Figure 1. A typical ECLipse digital circuit.

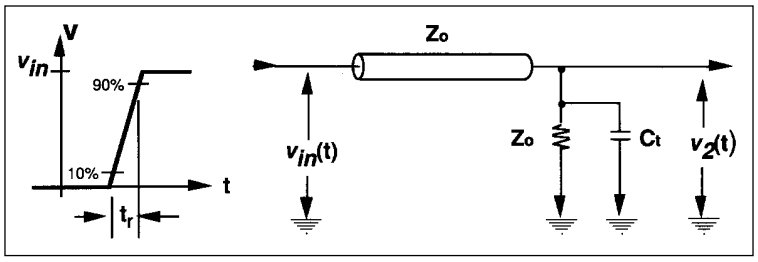


Figure 2. ECLipse transmission line equivalent model.

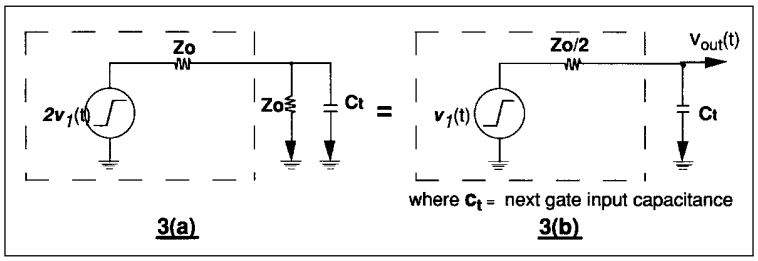


Figure 3. Thevenin equivalent models of Figure 2.

Table 1 shows the equivalent bandwidth for typical output risetimes from several fast logic families in addition to typical gate input capacitance values.

Digital circuit designers have a choice between transmission lines and conventional interconnect wiring when distances between gate devices are short. But what about adding the input capacitance of a probe to these high-speed circuits for device characterization or device testing purposes? The design decision must take into consideration additional lumped capacitance. Incorrect selection of measurement probe capacitance values could result in false system operation due to a high percentage of incident pulse reflections and subsequent lowering of the AC noise immunity. The basic factors which will affect this design decision are:

- System risetime
- Interconnect distance
- Capacitive loading (fanout plus probe lumped capacitance)
- Resistive loading (line termination)
- Percentage of undershoot and overshoot permissible (reduction in noise immunity)

Figure 1 represents a typical ECL logic circuit for the purpose of analyzing the degree of measurement error introduced by the probe. Remember that probe loading effects on a DUT become more pronounced as signal edge speeds get faster and propagation delay times become shorter. The variation of signal propagation times through a fast logic family versus the number of load gates is typically designed to meet very stringent system operating requirements in speed, skew, and circuit density.

The output waveform at the end of a parallel-terminated transmission line, shown as v_{load} in Figure 1 can be derived from an equivalent circuit using Thevenin's Theorem. Figure 2 shows the parallel-terminated transmission line circuit, along with the waveform driving the line.

Notice the transmission line is parallel terminated by Zo to ground with a capacitive load C_t. Figure 3a and 3b illustrate Thevenized versions of Figure 2.

The capacitive load, C_t serves to represent the DUT input capacitance plus any other capacitance that may present itself at the v_{out} node. Propagation delay increases through the transmission line may now be determined by changing Figure 3b into a simple time constant circuit with a time constant t_c and a series impedance Z_t. Under a no-load state, C_t = 0, the signal delay between the 50%-point of the input waveform and the 50%-point of the output waveform, is defined as the line delay, t_{pd}. See Figure 4.

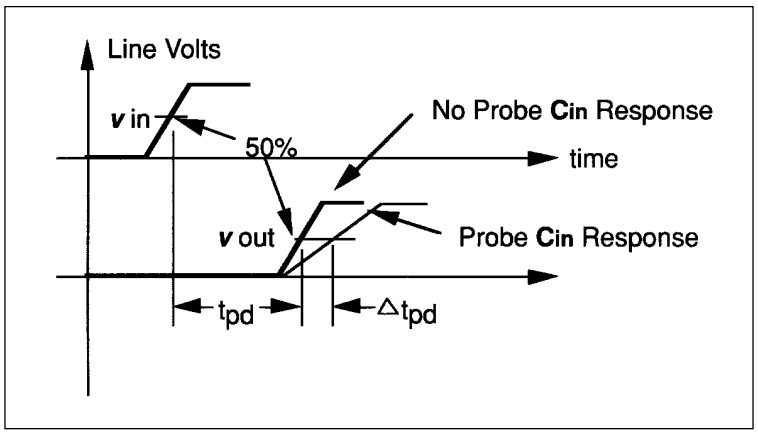


Figure 4. Δt_{pd} Introduced by the input capacitance of a measurement probe load.

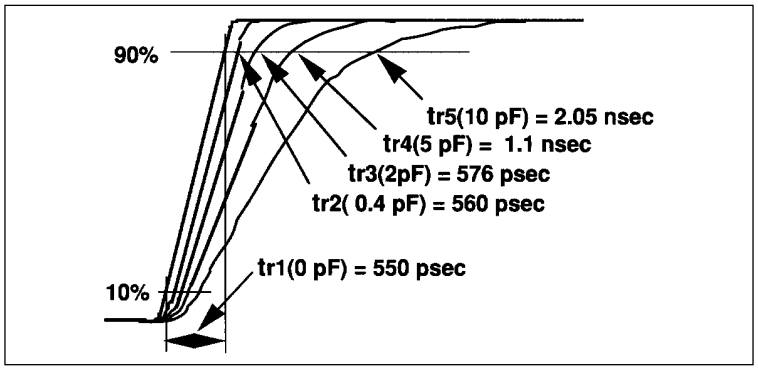


Figure 5. Effect of probe input capacitance on typical ECLipse logic signal risetime.

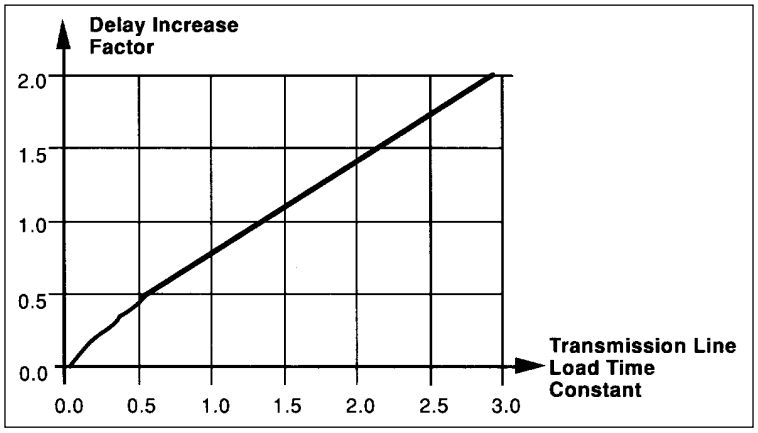


Figure 6. Signal delay increases as a function of probe input.

The capacitive load from a probe added to the end of the transmission line slows down the output signal risetime, thereby increasing t_{pd} by the amount Δt_{pd}. Figure 5 shows the increase in response delay for several different probe input capacitance loads.

The increase in signal risetime and signal delay as a function of additional lumped capacitance can be determined by the delay change and the time constant of the transmission line load. Figure 6 shows the relationship between the transmission line load time constant and the resulting change in delay.

This diagram gives a convenient graphical approximation for determining increases in signal delay as a function of additional lumped capacitive loads. The following example serves to illustrate the usefulness of the diagram.

Referring back to Figure 2, the transmission line is parallel terminated by 50 Ω driving an incremental 2 pF probe input capacitance load with a no-load risetime of 300 psec. The delay increase factor is determined by Figure 6. The transmission line load time constant is expressed by:

$$Ro * C_t/t r$$

Where:

$$Ro = Zo.$$

So:

$$RoC_t/t r = (50)(2 E-12)/300 E-12) = 0.33$$

Using this result and Figure 6, the transmission line load delay factor equals 0.36.

Therefore:

$$\Delta t_{pd} = (0.36)(300 psec) = 108 psec$$

The 108 psec is added to the no-load transmission line risetime to arrive at the approximate delay caused by a 2 pF lumped load at the output of the line. The 2 pF lumped capacitive load represents the incremental load of a medium performance active FET probe when used to pick off the digital signal at the point of interest. Table 2 shows the percent of measurement error introduced by a series of high-performance probes with different input capacitance values.

Table 2. Probe Measurement Error Introduced to a Typical ECLipse Logic Circuit Output Signal by the Input Capacitance of the Probe Measuring the Signal

Probe Input Capacitance	RoCt/tr	Δt_{pd}	Measurement Error in %	Probe Type
0.15 pF	0.025	9 psec	3	Tektronix P6150 Probe
0.4 pF	0.07	24 psec	8	Tektronix P6207/P6217 Active FET Probes
0.6 pF	0.10	45 psec	15	HP 54701A Active Probe
1.0 pF	0.17	51 psec	17	Tektronix P6156 Zo Probe
1.0 pF	0.17	51 psec	17	Tektronix P6243/P6245 Probe
2.0 pF	0.33	105 psec	35	Tektronix P6205 FET Probe
3.0 pF	0.50	120 psec	40	Tektronix P6201 FET Probe (1X)
8.0 pF	1.33	300 psec	100	Tektronix P6139A Passive Probe

Conclusion

The effect of probe input capacitance on signal risetime and propagation delays must be considered when selecting a probe for use with high performance integrated circuit logic technologies, such as Advanced CMOS, Fast ECL (e.g., ECLipse), and GaAs. The increase in propagation delay can be found by Theveninizing the DUT and converting the equivalent to a single time constant circuit with a step-function input voltage with a finite risetime voltage.

Thus, when critical delay paths and risetimes are being designed it must be compulsory for the designer to give special forethought to the circuit termination scheme and the method by which signals may be acquired with minimal impact to the optimization of the signal delay and risetime performance.

Therefore, the effect of incremental probe input capacitance on typical high-performance logic family gate-to-gate signal delay and risetime is to increase the propagation delay and slow down the signal risetime. To obtain the least measurement error and lowest propagation delay as a function of probe loading, the lowest characteristic probe input capacitance should be used.

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